

Introduction

This is radix-16 Viterbi detector core being developed for PRML(Partial Response Maximum Likelihood), which is widely used in HDD/ODD read channel signal processing. Based on our original ACS and pass memory algorithm, both of small-size and low-latency is achieved at the same time.

Four kinds of products are selectable to meet different demands.

Product No	Type	Soft-Output
Si2540	Small-size	No
Si2540-H	High-speed	No
Si2540-S	Small-size	Yes
Si2540-HS	High-speed	Yes

Features

- Simplified ACS loop for high-speed design
- Radix-16
- 8-State
- PR(Partial Response) transfer function configurable

$$G(D) = PR_A + PR_B \cdot D + PR_C \cdot D^2 + PR_D \cdot D^3$$

- Traceback length configurable
- Support soft-output
- Available two type : small-size, high-speed
- Low latency
- Fully synchronous design using a single clock
- ASIC friendly design

Deliverables

- Verilog-RTL source code
- FPGA netlist (Xilinx, Altera, Lattice etc.)
- ASIC netlist (need ASIC cell library)
- CPU/DSP source code (C, Assembler)

Test bench and test patterns are also provided.

Gate Count / Performance

- TSMC 65nmLP

Product No	Si2540	Si2540-H
Gate Count	206Kgate	285Kgate
Frequency	500MHz	555MHz
Latency	56sample	64sample
Data Rate	2Gbps	2.2Gbps

(n=6, m=5, traceback length=20)

Experience

- Successfully adopted in ASIC

Interface

	Name	Description
Input	ICLK	Clock
	IXRST	Asynchronous reset
	IDATA0[n-1:0]	Input data (t)
	IDATA1[n-1:0]	Input data (t-1)
	IDATA2[n-1:0]	Input data (t-2)
	IDATA3[n-1:0]	Input data (t-3)
	IPR_A[m-1:0]	PR transfer function A
	IPR_B[m-1:0]	PR transfer function B
	IPR_C[m-1:0]	PR transfer function C
	IPR_D[m-1:0]	PR transfer function D
Output	ODATA[3:0]	Detected data
	OSDATA0[s-1:0]	Soft-output (t) (*1)
	OSDATA1[s-1:0]	Soft-output (t-1) (*1)
	OSDATA2[s-1:0]	Soft-output (t-2) (*1)
	OSDATA3[s-1:0]	Soft-output (t-3) (*1)

*1 : Only for Si2540-S, Si2540-HS

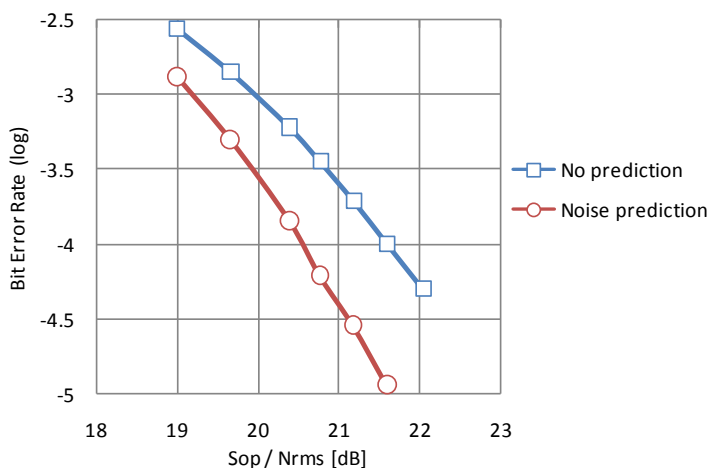
Applications

- Hard disk drive, Optical disc drive

Customization

- Change radix (Radix-2, Radix-4, Radix-8 etc.)
- Change number of state (4-State, 16-State etc.)
- Add data dependent noise prediction (below figure)
- Add signal distortion compensation

Effect of data dependent noise prediction



The content might change without a previous notice due to the improvement.

Please contact us for further works such as IP customization and peripheral circuit design.

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