Viterbi Decoder (Soft Decision Supported)

SIGLEAD

Introduction

This is high-speed soft decision viterbi decoder core, which is widely used as the decoder of convolutional code. The architecture without using external RAM is adopted. Working with our depuncture IP, various code rate is available (2/3, 3/4, 4/5, 5/6, 6/7, 7/8 etc). Four kinds of products are selectable to meet different demands.

Product No	Code Rate	Soft-Output
Si2530	1/2	No
Si2530-R3	1/3	No
Si2530-S	1/2	Yes
Si2530-R3S	1/3	Yes

Features

- Simplified ACS loop for high-speed design
- Convolutional code generator polynomial configurable
- Convolutional code constraint length (K) : >= 3
- Soft input data bit width (m) configurable
- Available hard input viterbi decoder (m=1)
- Support punctured convolutional codes
- Traceback length (t) configurable
- Support trellis initialization
- Support various trellis termination method
  (trellis termination, tail biting etc.)
- Path metric bit width configurable
- Support soft-output
- Available two type : high-speed, low-latency
- Latency : high-speed type t + (K-1) + ceil(t / (K-1)) + 4
  low-latency type t + (K-1) + 4
- Available unsuccessive input data by enable control
- Fully synchronous design using a single clock
- ASIC friendly design
- Support various code rate by using depuncture IP (Si2552)

Deliverables

- Verilog-RTL source code
- FPGA netlist (Xilinx, Altera, Lattice etc.)
- ASIC netlist (need ASIC cell library)
- CPU/DSP source code (C, Assembler)

Test bench and test patterns are also provided.

Applications

- Communications
  (support various standards with convolutional code)

Customization

- Change code rate (1/4, 1/5 etc.)
- Dynamically variable generator polynomial

Interface

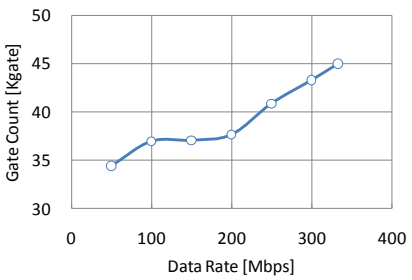
	Name	Description
Input	ICLK	Clock
	IXRST	Asynchronous reset
	IDATAG2[m-1:0]	Input data 2 (*1)
	IDATAG1[m-1:0]	Input data 1
	IDATAG0[m-1:0]	Input data 0
	IFORMAT	Input data format
	IPUNCG2	Puncture position 2 (*1)
	IPUNCG1	Puncture position 1
	IPUNCG0	Puncture position 0
	ITBLEN[1:0]	Traceback length
	ITLS[K-2:0]	Trellis initialization state
	ITLSINI[1:0]	Trellis initialization setting
	ITAILS[K-2:0]	Trellis termination state
	ITAILINI[1:0]	Trellis termination setting
	IDATAENB	Decode enable
	ISTART	Decode start (trellis initialization)
	IEND	Decode end (trellis termination)
Output	ODATA	Decoded data
	OSDATA[s-1:0]	Soft-output (*2)
	OVALID	Decoded data enable
	OFIRST	First decoded data
	OLAST	Last decoded data

*1 : Only for Si2530-R3, Si2530-R3S *2 : Only for Si2530-S, Si2530-R3S

Gate Count / Performance

- TSMC 90nm

(Constraints : Clock Skew 20%, Using wire load model)



Conv. code : (171,133)oct
K=7, m=5, t=48

50Mbps : low-latency type
100Mbps - : high-speed type

Gate Count : 2-NAND

- Xilinx Virtex-5 (XC5VLX30-3)

(Si2530, Conv. code : (171,133)oct, K=7, m=3, t=48)

high-speed type	Slice : 1571	Block RAM : 0	200Mbps (200MHz)
low-latency type	Slice : 937	Block RAM : 0	30Mbps (30MHz)
	Slice : 1226	Block RAM : 0	100Mbps (100MHz)

The content might change without a previous notice due to the improvement.

Please contact us for further works such as IP customization and peripheral circuit design.

SIGLEAD Inc.
1-38-10-203 Nakagawachuo Tsuzuki-ku
Yokohama-city Kanagawa-ken
224-0003, Japan

Contact and Ordering Information
TEL/FAX : 045-509-1885
E-mail : info@siglead.com

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http://www.siglead.com