NAND Flash Memory Controller

SIGLEAD

Introduction

si2590

This NAND flash memory controller supports SLC/MLC/TLC. Two different types are available: host CPU type and AMBA (AXI/AHB/ APB) type. The number of NAND interface channel can be customized according to customer's request; hence it's possible to support wide range of read/write speed.

Moreover, a total solution including firmware for such important functions like Bad Block Management, Wear Leveling (Dynamic/ Static), Garbage Collection, etc., can also be provided.

Features

- NAND type : SLC/MLC/TLC, 8bit/16bit
- NAND vendor : Toshiba/Micron/Intel/Samsung/Hynix/others
- NAND interface :
- ONFi Asynchronous/ONFi Synchronous/Toggle DDR
- NAND block size : 64 to 512 pages
- NAND page size : 2 to 16K Bytes
- Number of ECC (BCH) correctable bits : 1 to 256 bits
- Interleave supported
- Encryption (AES/DES) available as option
- Firmware available as option

Including Bad Block Management,

Wear Leveling (Dynamic/Static), Garbage Collection, etc.

- Deliverables
- Verilog RTL source code
- FPGA netlist (Xilinx, Altera, Lattice, etc.)
- ASIC netlist (need ASIC cell library)

Test bench and test patterns are also provided.

Evaluation Environment

A total evaluation environment with evaluation board & firmware is available on customer's request. Siglead will fully support customers to achieve the quick start of evaluation.

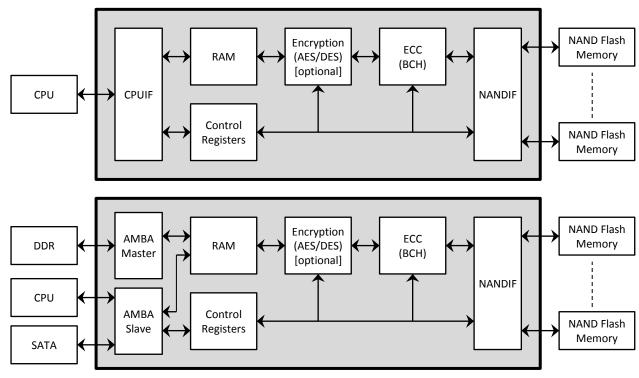


Customization

- Siglead will propose optimized architecture based on customer's request/specification such as number of channel, CE number, capacity, read/write speed etc.

- Siglead's original ECC technologies are available as an option.

Siglead is a leading company on signal processing/ECC technology for higher reliability and longer lifespan of products. Part of the developed technologies has been presented in international conference (ISSCC, FMS). Please contact us for more information.



The content might change without a previous notice due to the improvement.

Please contact us for further works such as IP customization and peripheral circuit design.

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Block Diagram