

Introduction of SIGLEAD

SIGLEAD Inc.

www.siglead.com

info@siglead.com

1. SIGLEAD Profile

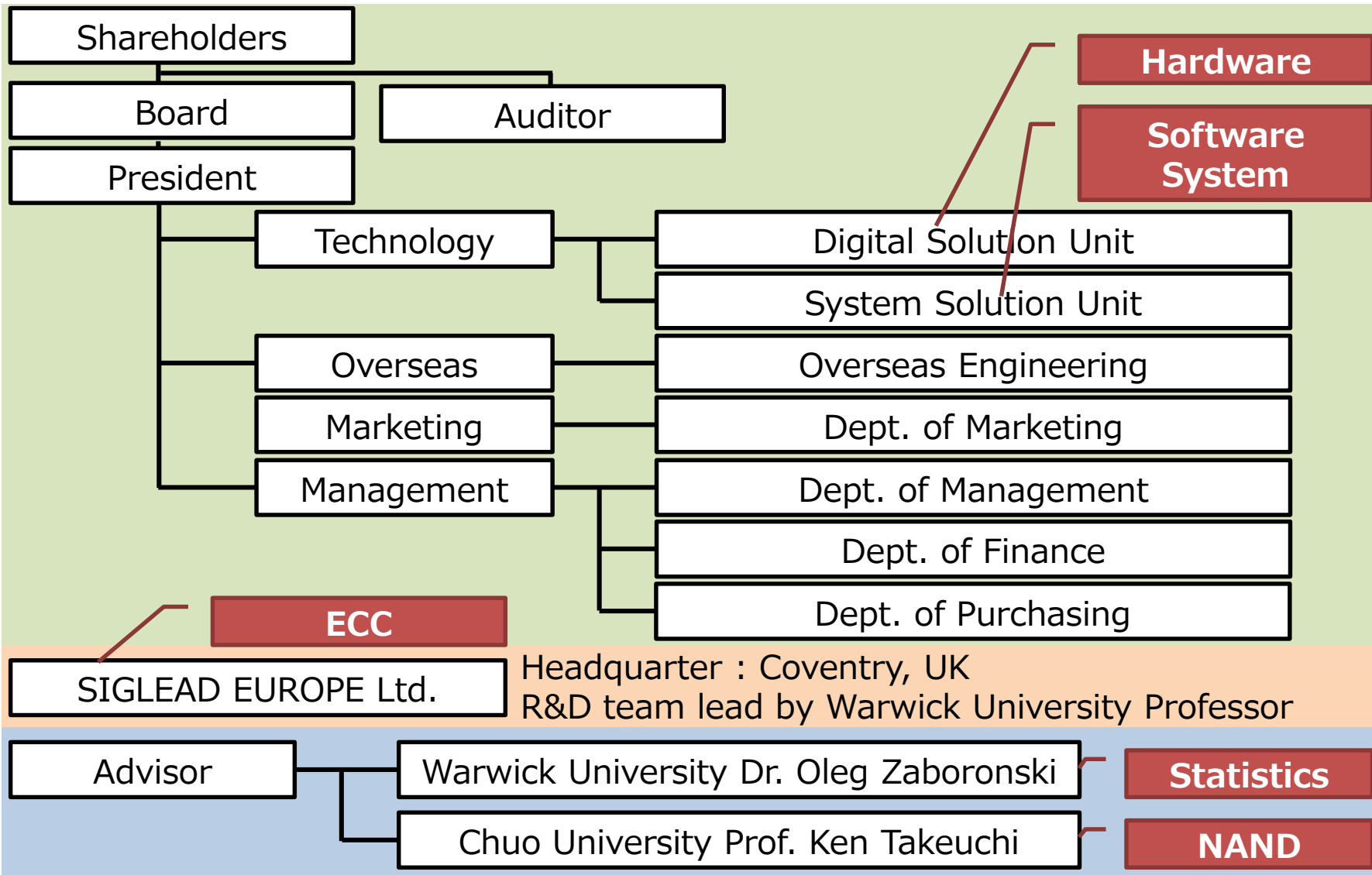
Company Overview / Organization
Technical Team / Core Competence
Business Territory

Company Overview

Name	SIGLEAD Inc.
Headquarter	Yokohama-city Kanagawa-ken, Japan
President	Atsushi Esumi (President & CEO)
Web Site	http://www.siglead.com
Establishment	February 5, 2007
Paid-in Capital	183million Japanese Yen
Shareholders	VC, Hon Hai Technology Group, Co-founders
Executives	Atsushi Esumi, Ichiro Myochin, Kazuo Migita Yuichiro Saito
Total Members	17
Locations	Headquarter : Yokohama-city Kanagawa-ken, Japan SIGLEAD EUROPE Ltd. : Coventry, United Kingdom SIGLEAD Taiwan Office: Hsinchu, TaiWan.



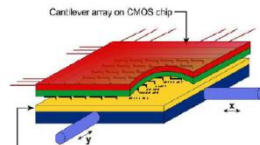
Organization



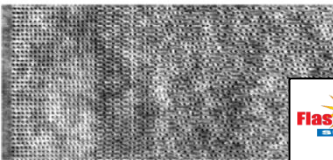
Technical Team

- ✓ Highly experienced researchers / engineers from Toshiba, Rohm, Sony, TI, Fujitsu, Warwick University, etc.
- ✓ An international research team with more than 20 years of averaged experience in R&D of signal processing algorithm for data storage.
- ✓ Around 80 patents in Japan, USA and UK registered as the inventors.
- ✓ Full capability of algorithm, IC design, firmware and sales.

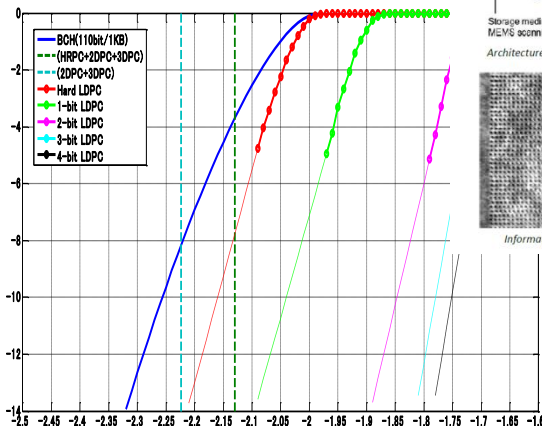
ProTem Project



Storage medium on MEMS scanner
Architecture of the "Millipede" concept (Figure courtesy IBM Zurich)



Information recorded at 1Tb/in² (Figure courtesy IBM Zurich)

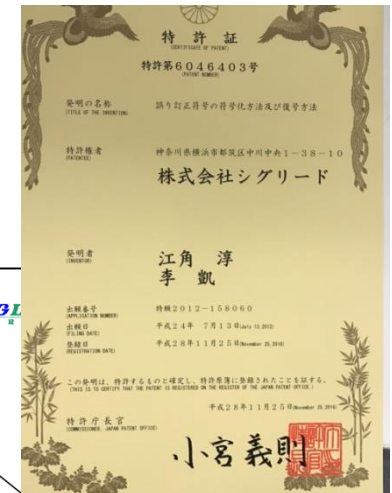


- Siglead Europe participated in the ProTem project
 - 4 year EC-funded project
 - Partners: University of Exeter, IBM Zurich, Numonyx, CEA LETI, Fraunhofer ISIT, RWTH-Aachen, University of Twente, Plarion
 - Aim: To develop probe storage micro-nano techniques and systems for ultra-high capacity, low power, small form-factor memories, with a particular focus on archival and backup applications.
- Common to all proposal for probe storage systems is an array of thousands of AFM probes reading and writing in parallel

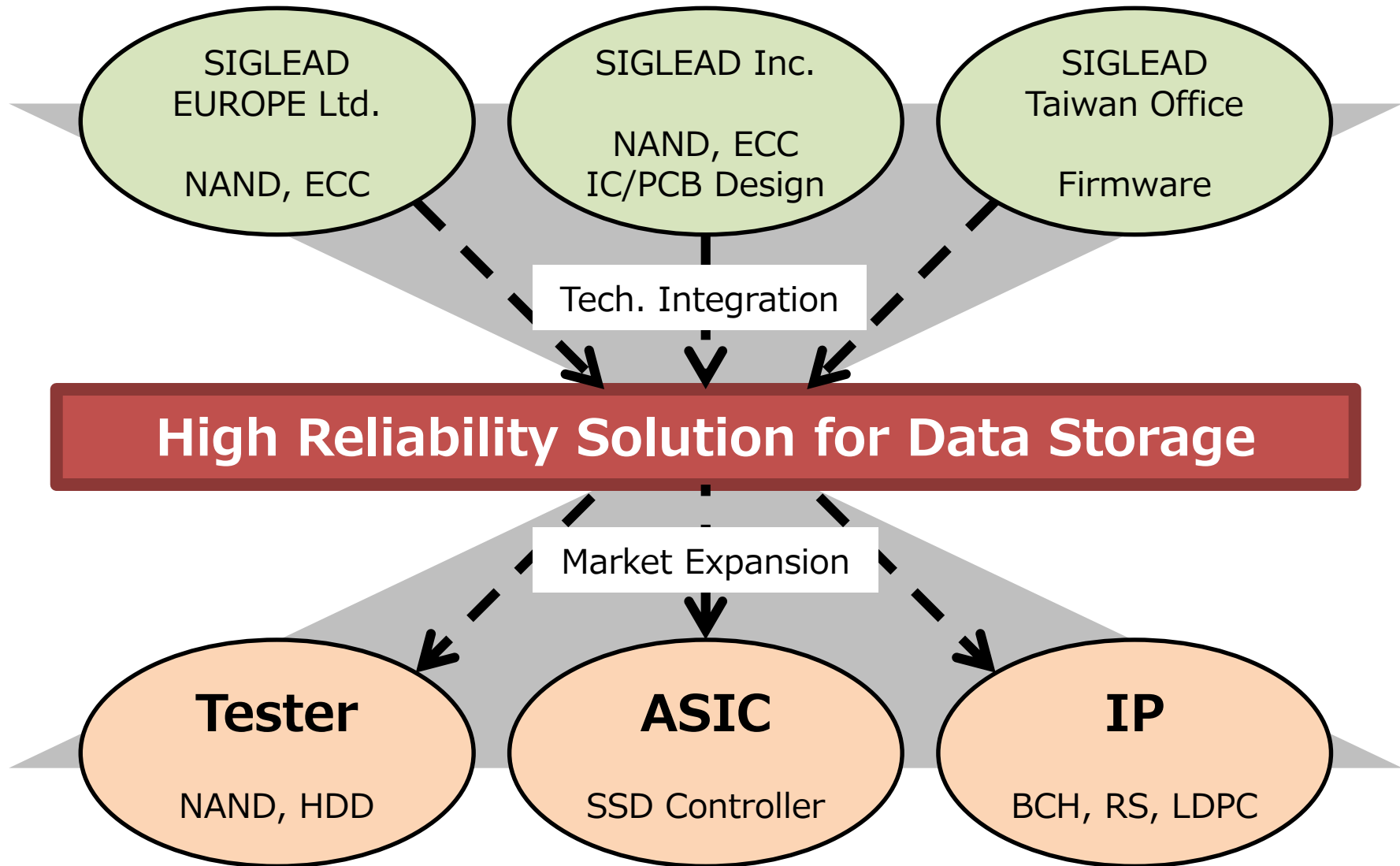
Flash Memory SUMMIT

“High Radix” LDPC: Tanner Graph

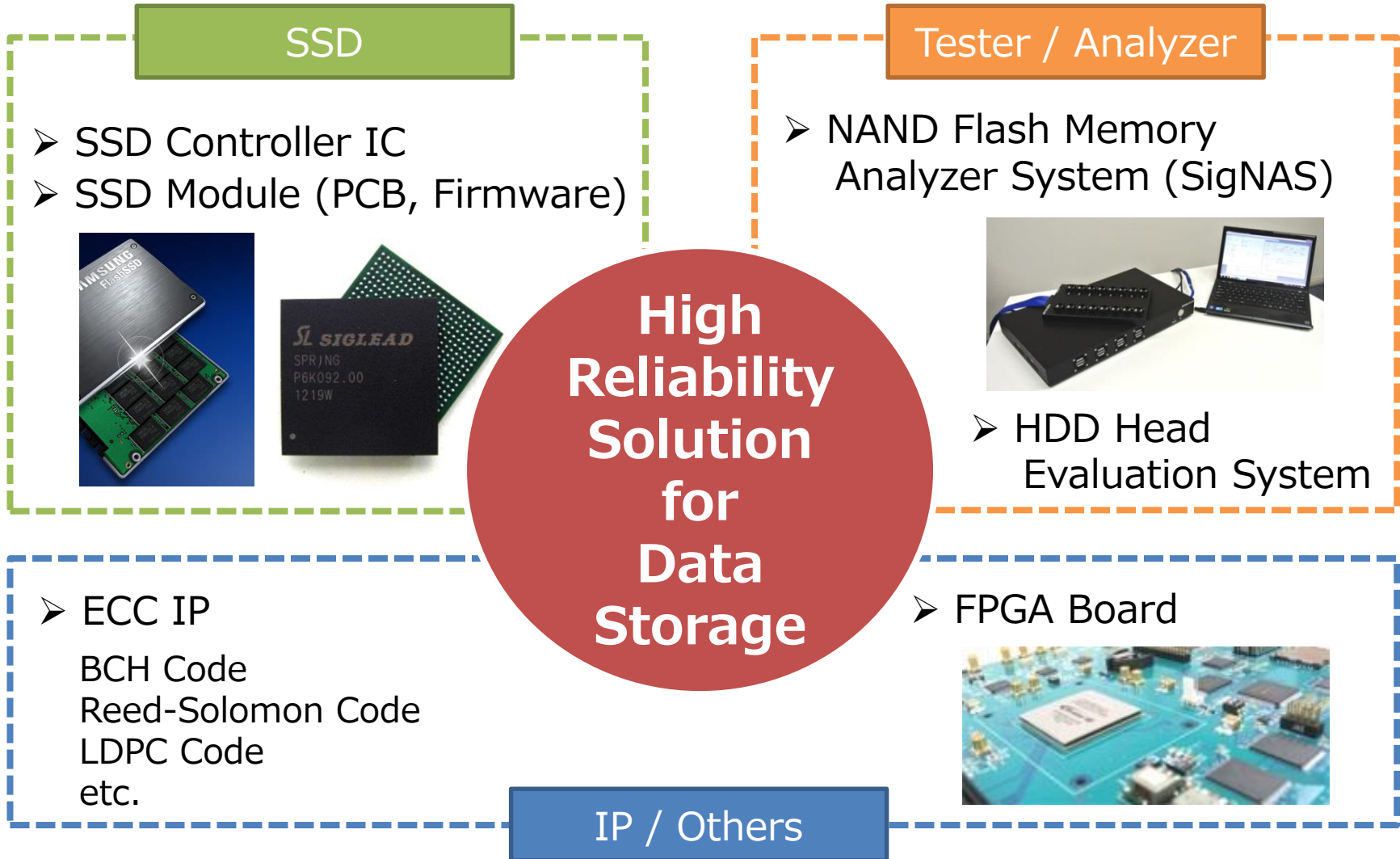
merge variable/check nodes of binary LDPC...



Core Competence



Business Territory



2. SSD Controller IC

Line-up / Example of New ECC
Original Error Correction Technology
ECC Evaluation (Endurance, Data Retention)
Customer's News Release
Firmware / SSD Module Testing Result

Achieved Mass Production, Adopted by SONY



Line-up



Planning

Consumer
PCIe SSD

Planning

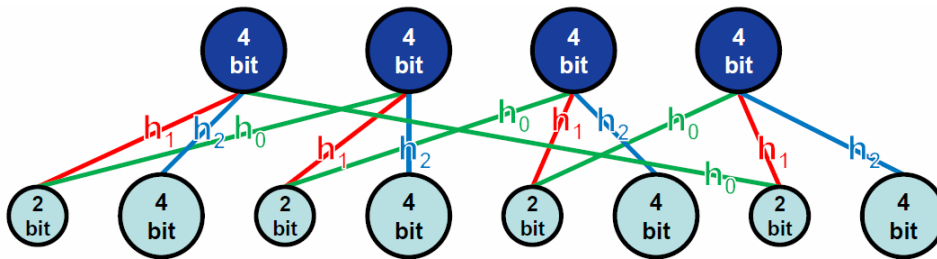
Enterprise
PCIe SSD

	SL2007DH	STYLUS	STYLUS
Process Node	65nm LP	40nm or 28nm	28nm
Channel	8	4	8
Package	441ball BGA	225ball FC-BGA	461ball FC-BGA
Sequential Read	550MB/s	T.B.D	T.B.D
Sequential Write	520MB/s	T.B.D	T.B.D
4K Random Read	360MB/s	T.B.D	T.B.D
4K Random Write	310MB/s	T.B.D	T.B.D
Cache	DDR3 Max.1GB	DRAM less	DDR4
Host I/F	SATA3 (6.0Gbps)	PCIe Gen3 x2 (NVMe)	PCIe Gen3 x4 (NVMe)
ECC	BCH + HRPC + 2DPC + 3DPC + WCC	BCH or LDPC based SIGLEAD original	BCH + LDPC based SIGLEAD original
Encryption	AES 128bit / 256bit	AES 128bit / 256bit	AES 128bit / 256bit
Wear Leveling	dynamic / static	dynamic / static	dynamic / static
CPU	32bit RISC	Undisclosed	Undisclosed
TLC / 3D NAND	Supported	Supported	Supported

Example of New ECC (Implemented in SL2007D)

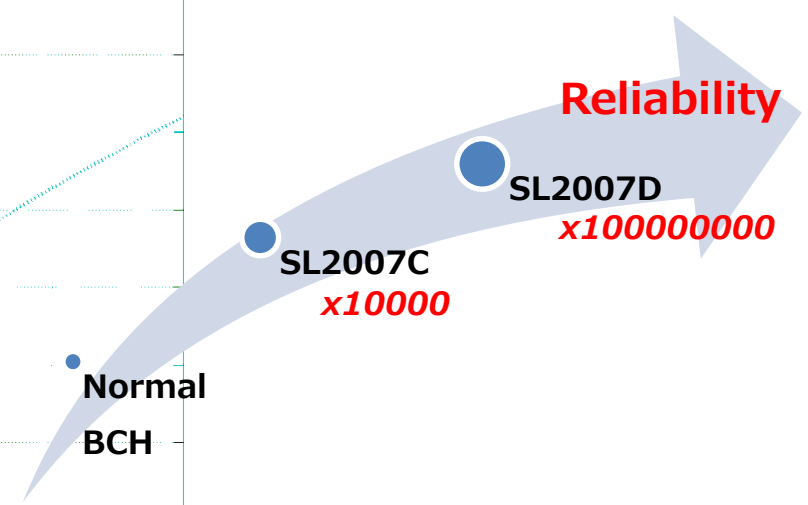
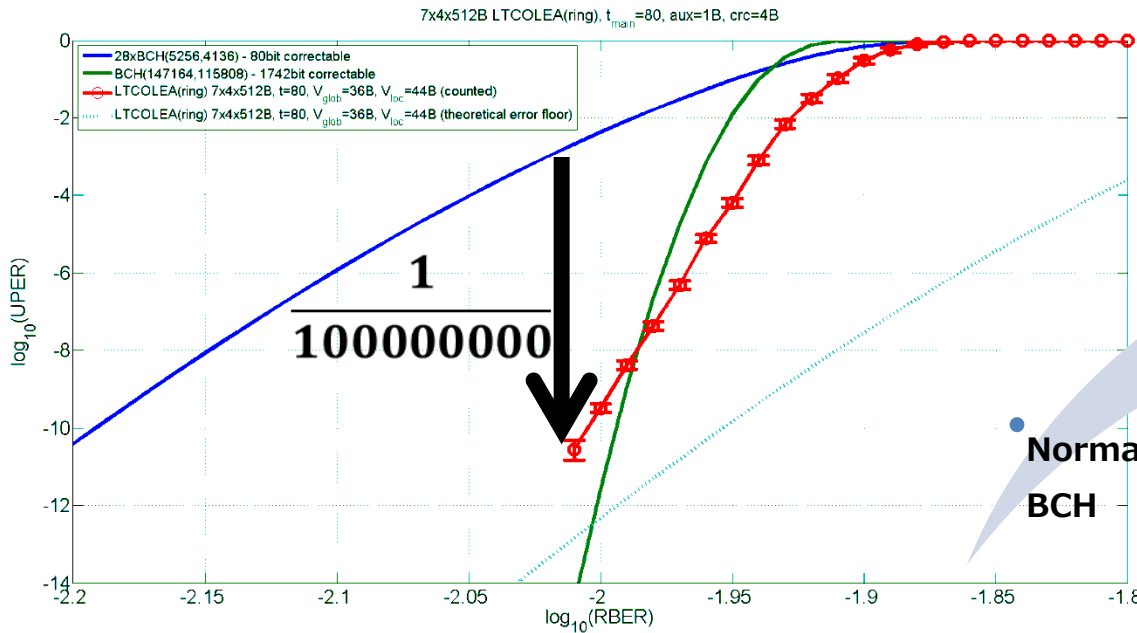
New Technology1: High Radix LDPC Like Code

New Technology2: Cascade Decoding



$$H = \begin{bmatrix} h_1 & h_2 & 0 & 0 & 0 & 0 & h_0 & 0 \\ h_0 & 0 & h_1 & h_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & h_0 & 0 & h_1 & h_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & h_0 & 0 & h_1 & h_2 \end{bmatrix}$$

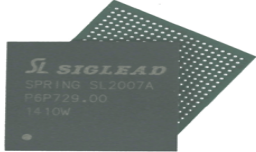

Please refer to FMS2015 (Flash Memory Summit) presentation for detail.



Original Error Correction Technology

Error number significantly reduced due to original technology


High reliability






 Siglead ECC & conventional NAND

BCH code & NAND Flash
 conventional NAND





 automobile


 medical equipment


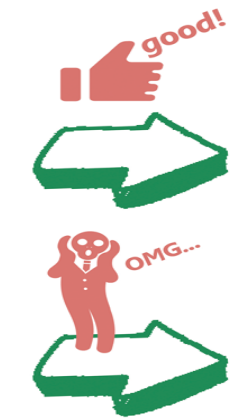
 industrial equipment


Low cost





 Siglead ECC & next generation NAND

BCH code & NAND Flash
 next generation NAND





 PC


 IT appliance

ECC Evaluation: Endurance/Data Retention (MLC)

Controller : SIGLEAD SL2007D

NAND Flash Memory : Toshiba, 15nm, MLC, TH58TFG9DFLBA8C, BGA132

(SIGLEAD ECC)

P/E cycle	Data Retention (month)		
	0	6	12
3,000	PASS	PASS	PASS
10,000	PASS	PASS	PASS
15,000	PASS	PASS	FAIL

(BCH)

P/E cycle	Data Retention (month)		
	0	6	12
3,000	PASS	PASS	PASS
10,000	PASS	FAIL	FAIL
15,000	FAIL	FAIL	FAIL

ECC Evaluation: Endurance/Data Retention (TLC)

Controller : SIGLEAD SL2007D, NAND Flash Memory : 2D-TLC
(SIGLEAD ECC)

P/E cycle	Data Retention (month)					
	0	6	12	24	36	48
300	PASS	PASS	PASS	PASS	PASS	PASS
600	PASS	PASS	PASS	FAIL	FAIL	FAIL
1,000	PASS	PASS	PASS	FAIL	FAIL	FAIL
1,500	PASS	FAIL	FAIL	FAIL	FAIL	FAIL
2,000	PASS	FAIL	FAIL	FAIL	FAIL	FAIL
3,000	PASS	FAIL	FAIL	FAIL	FAIL	FAIL

(BCH)

P/E cycle	Data Retention (month)					
	0	6	12	24	36	48
300	PASS	PASS	PASS	FAIL	FAIL	FAIL
600	PASS	PASS	FAIL	FAIL	FAIL	FAIL
1,000	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
1,500	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
2,000	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
3,000	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL

SONY released its products based on Siglead solution

SONY お問い合わせ・サポート サイトマップ ソニーについて 検索 Japan

企業情報 ニュースリリース 投資家情報 CSR・環境・社会貢献 採用情報 デザイン ブランド

トップ > ソニーについて > ニュースリリース > 2016 > 業界最長クラスの寿命と高い信頼性を実現したSSDを製品化

ニュースリリース

English | コンテンツメニュー

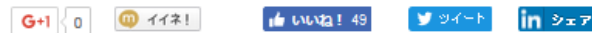
報道資料

ここに掲載されている情報は、発表日現在の情報です。
検索日と情報が異なる可能性がありますので、あらかじめご了承ください。

2016年08月25日

業界最長クラスの寿命※1※2と高い信頼性を実現したSSDを製品化

産業機器、組み込み用途に向けた外部記憶装置として



ソニー株式会社

ソニーストレージメディア・アンド・デバイス株式会社

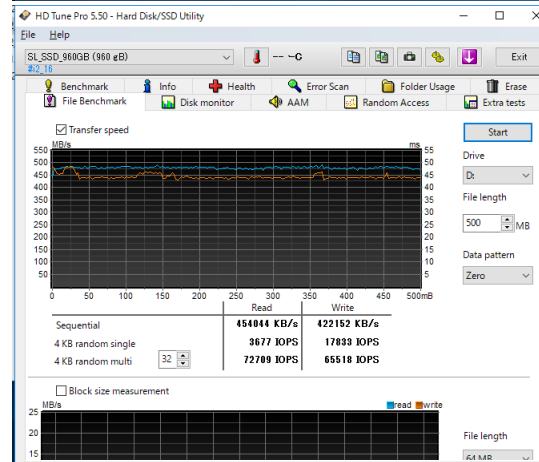
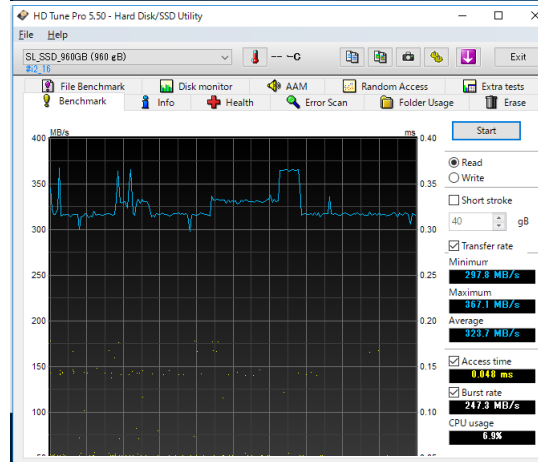
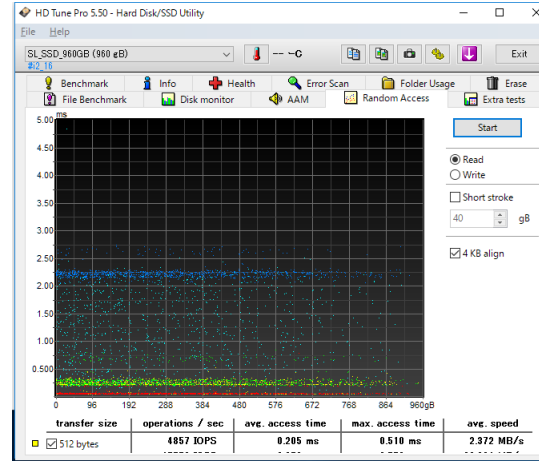
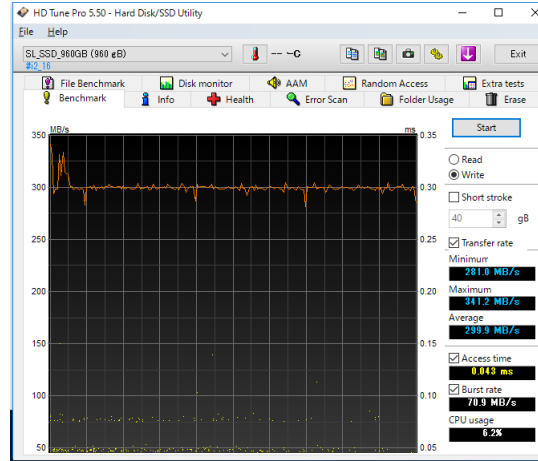
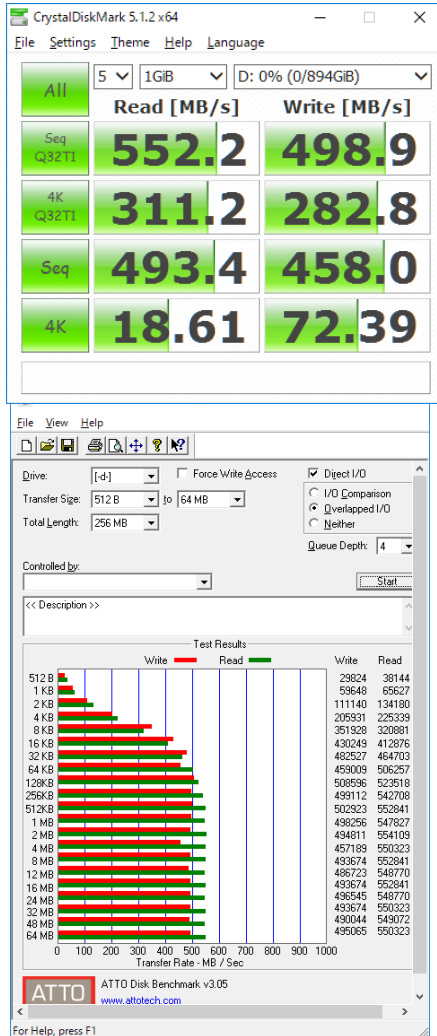
ソニーは、業界最長クラスの寿命※1※2と、電源遮断耐性と書き込み速度を維持することで、様々な使用環境において信頼性を高めたSSD（ソリッド・ステート・ドライブ）を、産業機器、組み込み用途に向けて製品化し、9月上旬よりサンプル出荷を開始します。



SONY's announced its leading SSD achieves longest life time

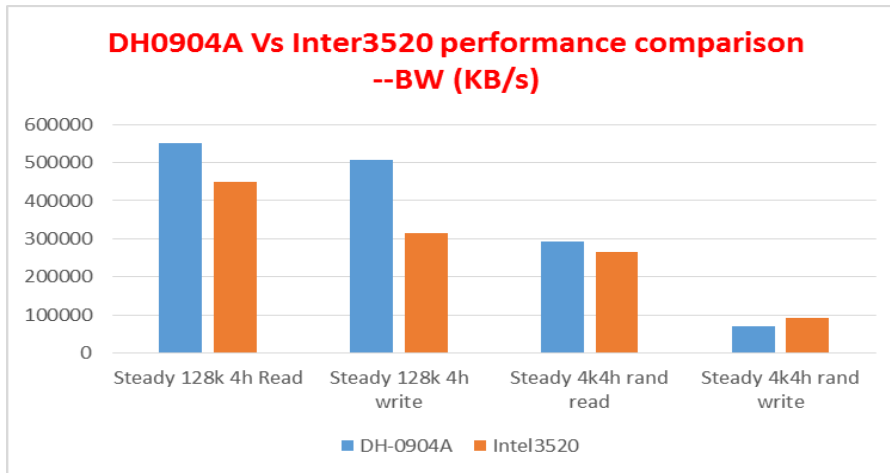
Firmware / SSD Module Testing Result (1)

For Industry: Stable read/write performance have been achieved.



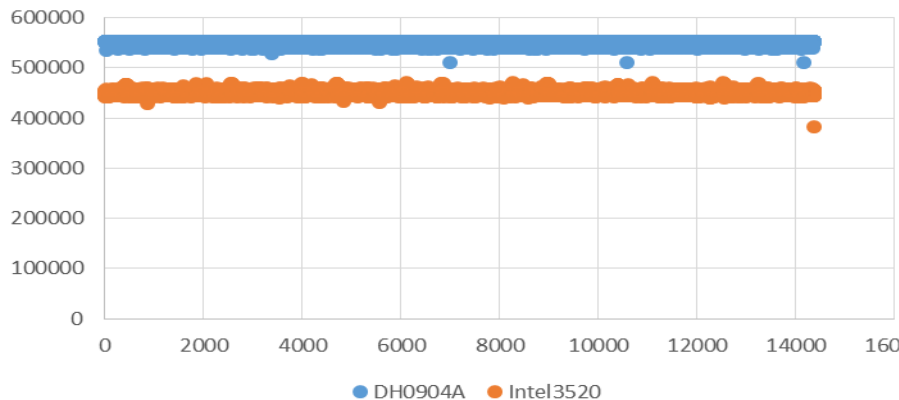
Firmware / SSD Module Testing Result (2)

For Server: Better or comparable performance have been achieved. (vs Intel 3520)

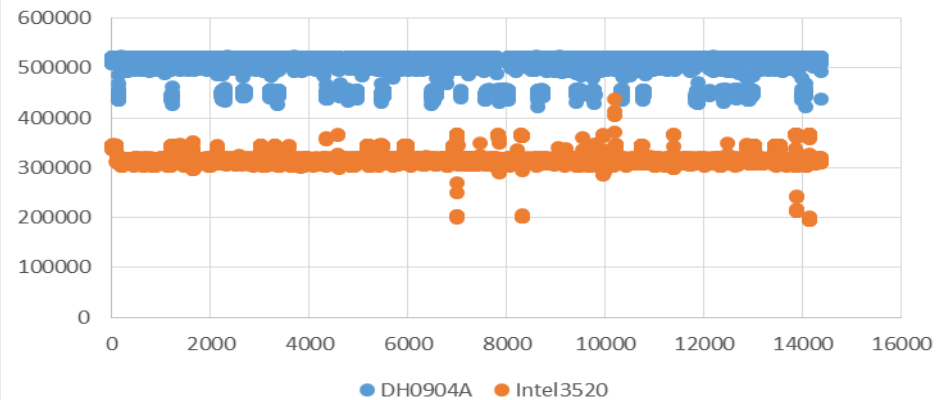


R/W Performance after 1 hour 128K Sequential Write

Comparison of 128k 4h read test



Comparison of 128k 4h write test



3. NAND Analyzer System

NAND Flash Memory Tester SigNAS3 • SigNASII
Customer of SigNAS Series

NAND Flash Memory Tester - SigNAS3

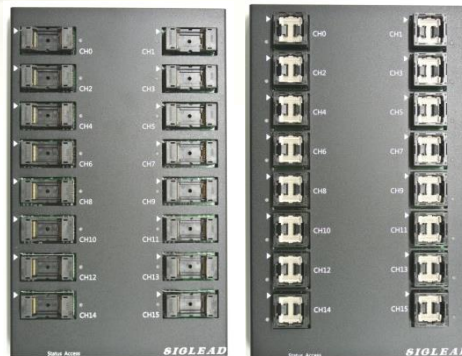
Catalog is available.
<http://www.siglead.com>

New products based on SigNASII, capable of testing up-to 128 NAND simultaneously with advanced analyzing features. Suitable for massive number of NAND acceptance inspection and data acquisition.

Size	Main-board 304.5mm x 498.5mm x 51.5mm Sub-board 279mm x 173mm x 45mm
Power Supply	AC:90V~264V (DC:15V/40A)
Power Consumption	360W (with 8 Sub-boards)
NAND number	Max. 128 (with 8 Sub-boards)
I/F	USB2.0, USB3.0, Giga Ethernet
Storage Temperature	Main-board -40~105°C Sub-board -40~105°C
Operating Temperature	Main-board 0~55°C Sub-board -40~85°C



Main Board



Sub Board - TSOP48

BGA152

< Deliverables >

- Main-board, Sub-board
- Cable, Power unit
- Analysis software
- NAND controller and firmware (implemented in Main-board)
- Operational guide

NAND Flash Memory Tester - SigNASII

Catalog is available.
<http://www.siglead.com>

Easy-to-use NAND analyzer system, provides operation verification of NAND flash memory from various vendors, error analysis, detailed error cause analysis, measurement of ECC performance, etc.

< Part of features >

- Error rate measurement (bit error rate, page error rate after ECC)
- Measurement of data retention, program disturb, read disturb
- Analysis of error distribution (page dependence, column dependence)
- Program pattern setting (increment, pseudo random, page stripe, etc.)
- Access time measurement
- Script execution to enable flexible measurement

< Deliverables >

- Mother board, Daughter board
- Analysis software
- NAND controller and firmware (implemented on Mother board)
- Operation manual



Customer of SigNAS Series

HITACHI
Inspire the Next

SONY®

FUJITSU



Panasonic



AVAGO
TECHNOLOGIES

SIEMENS

KEYENCE FANUC

Tech
Insights



東京大学
THE UNIVERSITY OF TOKYO

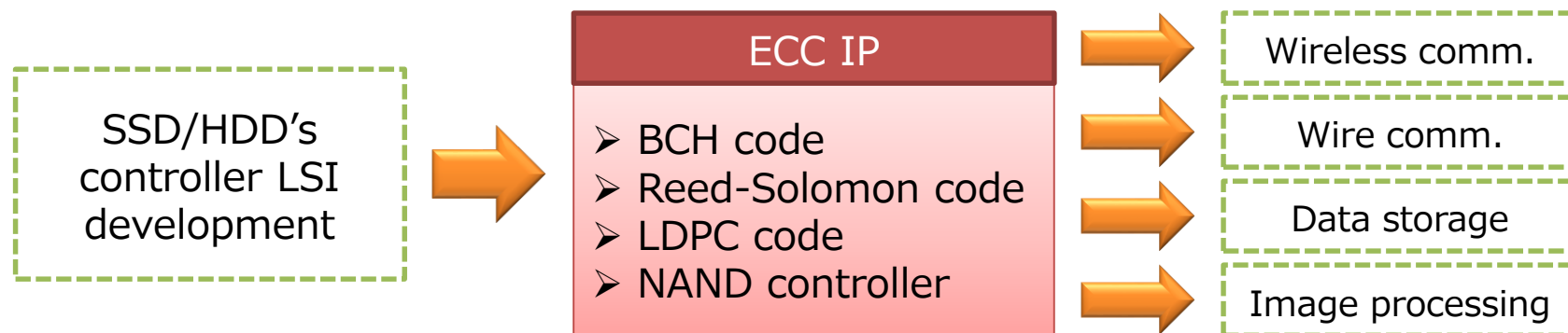
4. Other Products

Error Correction IP
Signal Processing FPGA Board

Error Correction IP

Catalog is available.
<http://www.siglead.com>

Error correction IP based on the development of SSD/HDD controller LSI
 Widely applicable to communications, optical storage and flash memory etc.



< Deliverables >

Several kinds of deliverables can be provided to meet customer's request

- Licensing of IP - RTL source code - FPGA netlist - ASIC netlist
- CPU/DSP source code etc.

IP customization and peripheral circuit design are also available.

Signal Processing FPGA Board

Catalog is available.
<http://www.siglead.com>

- Original FPGA board with high-speed AD/DA
- Suitable for high-speed signal processing and high-speed communication

FPGA	Altera StratixIV
ADC	12bit 1Gsps 8-channels
DAC	14bit 2.4Gsps 4-channels
Memory	DDR3 SDRAM 204pin Unbuffered SO-DIMM (Max 4GByte)
I/F	USB2.0 : B connector (x1) SMA connector for transceiver : TX/RX 16pair (Max 8Gbps) MICTOR connector for logic analyzer (32 user pins) DIP switch (x16) Push button (x1) LED (x8)

Customization is also available.

[Customization example]

- FPGA board with 8bit 5Gsps ADC
- FPGA board with 16bit 105Msps ADC 18-channels
- FPGA board with WiFi module
- FPGA with 5GHz OFDM signal generator

Signal Processing FPGA Board

Catalog is available.
<http://www.siglead.com>

